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APPLICATION NO.	F	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,960	•	04/15/2004	Daniel J. Ferris	X-1016 US	7471
24309	7590	04/27/2006		EXAMINER	
XILINX, II	NC		TON, MY TRANG		
ATTN: LEGAL DEPARTMENT 2100 LOGIC DR			ART UNIT	PAPER NUMBER	
SAN JOSE, CA 95124				2816	
				DATE MAILED: 04/27/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	10/824,960	FERRIS, DANIEL J.	
Office Action Summary	Examiner	Art Unit	
	My-Trang N. Ton	2816	
The MAILING DATE of this communication app Period for Reply		orrespondence address	
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from 1, cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).	
Status			
1) Responsive to communication(s) filed on			
	action is non-final.		
3) Since this application is in condition for allowar		secution as to the merits is	
closed in accordance with the practice under E	•		
	n parto Quayro, 1000 O.D. 11, 10	00 0.0. 210.	
Disposition of Claims			
4)⊠ Claim(s) <u>1-25 and 27-30</u> is/are pending in the a	application.		
4a) Of the above claim(s) is/are withdraw	vn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>1-25 and 27-30</u> is/are rejected.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and/or	r election requirement.		
Application Papers			
9) The specification is objected to by the Examine	r		
10)⊠ The drawing(s) filed on <u>04 August 2005</u> is/are:		to by the Examiner.	
Applicant may not request that any objection to the			
Replacement drawing sheet(s) including the correct		` '	
11) The oath or declaration is objected to by the Ex			
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign	priority under 35 H S C & 110(a)	a-(d) or (f)	
a) All b) Some * c) None of:	phonty under 33 G.G.C. § 119(a)	-(u) or (i).	
1. Certified copies of the priority documents	s have been received		
2. Certified copies of the priority documents		on No	
3. ☐ Copies of the certified copies of the prior	* *		
application from the International Bureau			
* See the attached detailed Office action for a list	` ',''	d Southandon	
		, _V V	
		MY-TRANG NUTON PRIMARY EXAMINER	
Attachment(s)			
1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)	
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	ate	
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal P 6) Other:	atent Application (PTO-152)	

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DETAILED ACTION

In view of newly discovered prior art, new ground of rejection are now set forth.

Any inconvenience caused by the delay in citing this new prior art is regretted.

Claim Rejections - 35 USC § 112

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites the limitation "the load" in last line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8, 11, 14, 17-18, 20-25, 27-28 and 30 are rejected under 35

U.S.C. 102(b) as being anticipated by Khoury et al (U.S Patent No. 5,532,637).

Khoury et al disclose in figs. 3-4 a linear low-noise mixer including:

a differential amplifier (11, 12) for receiving and amplifying input signals (IN1+,

IN1-), the differential amplifier (11, 12) providing a predetermined gain to the input signals (IN1+, IN1-);

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a load (19, 20) for providing a load impedance;

a dual differential switching stage (15-18), coupled to the differential amplifier (11, 12) and the load (19, 20), the dual differential switching stage (15-18) mixing the amplified input signals (IN1+, IN1-) from the differential amplifier (11, 12) with a local oscillator signal (LOI+, LOI-) to produce an output signal (O/P+, -) at the load (19, 20); and

; a current modifier (25, 26), coupled to the differential amplifier (11, 12), the current modifier (25, 26) altering current in the differential amplifier (11, 12) to adjust current through the load (19, 20) (25-26 allow the current through 15-18 to be reduced and provide additional current to 11-12) as recited in claim 1.

Regarding claim 3: the current modifier (25, 26) comprises a current source (25, 26), coupled to the differential amplifier (11, 12), the current source (25, 26) injecting current into the differential amplifier (11, 12) to reduce current through the load (19, 20) by supplementing current in the differential amplifier (11, 12).

Regarding claim 4: the current source (25, 26) comprises a first (25) and second (26) current device, the first current device (25) being coupled to a first transistor (11) of the differential amplifier (11-12) and the second current device (26) being coupled to a second transistor (12) of the differential amplifier 11-12).

Regarding claim 5: the current source (25, 26) reduces the current flowing through the load (19-20) to enable a lower supply voltage.

Regarding claim 6: because the structure of the claim is fully met so the functional limitation is also met.

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Claim 7 is similarly rejected as claim 6.

Regarding claim 8: the differential amplifier (11, 12) comprises a first and second transistor (11, 12) differentially coupled having first electrodes joined at a common node (node between 13, 14).

Regarding claim 11: the dual differential switching stage (15-18) comprises a first differential transistor pair (15, 16) having first electrodes coupled at a first common connection (connected to 11) and a second differential transistor pair (17, 18) having second electrodes coupled at a second common connection (connected to 12), the first common connection being coupled to a second electrode of the first transistor (11) of the differential amplifier (11-12) and the second common connection being coupled to a second electrode of the second transistor (12) of the differential amplifier (11-12).

Claim 14 is similarly rejected as claim 11.

Regarding claim 17: the dual differential switching stage (15-18) comprises first (15, 16) and second (17, 18) differential pairs, the first and second differential pairs having output electrodes cross coupled (O/P+, -).

Claim 18 is similarly rejected as above claim 1: RF amplifier stage (11, 12), a mixer stage (15-18), a load (19-20) and a current modifier (25-26).

Claim 20 is similarly rejected as claim 3.

Claim 21 is similarly rejected as claim 4.

Claim 22 is similarly rejected as claim 5.

Claim 23 is similarly rejected as claim 6.

Claim 24 is similarly rejected as claim 7.

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Claim 25 is similarly rejected as claim 17.

The method recited in claim 27 is similarly rejected as claim 18.

Claim 28 is similarly rejected as claim 1: means for amplifying (11, 12), means for receiving (15-18) and means for injecting current (25, 26).

Claim 30 is similarly rejected as above claim: a differential amplifier (11, 12), first and second current sources (25, 26), a load (19, 20) and a dual differential switching stage (15-18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 9-10, 12-13, 15-16, 19, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury et as applied to claims above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Khoury et al. However, these limitation does not specifically show "the current modifier comprises a current sink" (claim 2), "first electrodes comprises sources... " (claim 9); "the current sink" (claim 19), "means for sinking current" (claim 29).

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Per limitation "the current modifier comprises a current sink" recited in claim 2, this appears to be obvious variations (i.e., not patentably distinct to the current sources 25-26). Therefore, it would have been obvious to one of ordinary skill in the art to employ (25-26 as current sinks), as they appear to be obvious variations (not patentably distinct) and yielding same functional device.

Regarding claim 9: field effect transistors are well-known switching devices and patentable equivalent to bipolar transistors (11-12) since no unobvious results are seen produce from there use. Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of transistors (11-12 be FETs have sources, drains & gates) because of this well-known advantages in performance and integration. FETs have very short switching times and very low electrical power consumption.

The same motivation applied to claim 9 is applied to claim 10.

The same motivation applied to claim 9 is applied to claims 12-13 regarding the limitations "source, drain".

The same motivation applied to claim 9 is applied to claims 15-16 regarding the limitation "source electrodes, drain electrodes".

The same motivation applied to claim 2 is applied to claim 19 regarding "a current sink".

Claim 29 is similarly rejected as above claims: means for amplifying (11, 12), means for receiving (15-18). The same motivation applied to claim 2 regarding "means for sinking current" applied to claim 29.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton Primary Examiner Art Unit 2816

April 20, 2006